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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/683,552	01/17/2002	Mark S. Styduhar	BUR920010094	8934
28211	7590	06/20/2005	EXAMINER	
FREDERICK W. GIBB, III MCGINN & GIBB, PLLC 2568-A RIVA ROAD SUITE 304 ANNAPOLIS, MD 21401			NGUYEN, HIEP	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 06/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/683,552

Applicant(s)

STYDUHAR, MARK S.

Examiner

Hiep Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 April 2005.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 21-40 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) _____ is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 35-40 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/ or clarification is required.

Regarding claim 35, the recitation “ by selective selection of either said input signal or ground signal through a plurality of transmission gate” is indefinite because it is not clear which part of the circuit is selected to have input signal or to have a ground voltage.

Claims 36-40 are indefinite because of the technical deficiencies of claim 35.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 21-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ono (US 2001/0007443A1) view of Ishii (US Pat. 6,886,066).

Regarding claim 21-23, figure 11 of Rose shows a comparator cycling between an analog configuration and a digital configuration comprising: at least two transistors (1), (2) switches (74) and (76) coupled to the transistors for selecting a reference voltage (71) and a comparator output. The comparator is set to trip point associated with the rising/falling edge of the input signal; a tail current source (3). The first and second trip points of the comparator is set externally and when one of the input signal is getting close to the trip point, the comparator function as an analog amplifier. When the trip point is reach, the output of the

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comparator change state and the comparator is in digital configuration. Figure 11 of Ono show that switches (74) and (76) are transmission gates. Figure 3D of Ishii shows switches formed by transmission gates for more flexible control. Therefore, it would have been obvious to an artisan having skills in the art to replace switches (74) and (76) of Ono with the transmission gate taught by Ishii for more flexible control. Note that in the digital configuration, the input signal is greater than the voltage of the reference voltage. At that time the comparator changes states. The trip point can be adjusted by adjusting the W/L ratio.

Regarding claim 24, it is inherent that every comparator performs with hysteresis (or Schmitt trigger). When the W/L ratios of the transistors are not equal, the asymmetric Schmitt triggering happens.

Regarding claims 25-27, the transistors comprise:

- a first transistor of length (Lx) and a width of (Wx); and

- a second transistor of length (Ly) and a width of (Wy),

- wherein, said width-to length ratio equals $(W_x V_y)/(W_y L_x)$, and

- the level of the input signal that causes the output of the comparator to change state depends on the width-to-length ratio and the first or second trip points can be changed by varying the W/L ratios.

Regarding claim 28, if the trip point and the reference voltage are selected to be low, it is inherent that the time the comparator is in the digital configuration can be large (80% or more of the cycle time).

Regarding claims 29-32, figure 11 of Ono shows a comparator cycling between an analog configuration and a digital configuration comprising: at least two transistors (1), (2) switches (74) and (76) coupled to the transistors for selecting a reference voltage (71) and a comparator output. The comparator is set to trip point associated with the rising/falling edge of the input signal; a tail current source (3). The first and second trip points of the comparator is set externally and when one of the input signal is getting close to the trip point, the comparator function as an analog amplifier. When the trip point is reach, the output of the comparator change state and the comparator is in digital configuration. Figure 11 of Ono show that switches (74) and (76) are transmission gates. Figure 3D of Ishii shows switches formed by transmission gates for more flexible control. Therefore, it would have been obvious

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to an artisan having skills in the art to replace switches (74) and (76) of Ono with the transmission gate taught by Ishii for more flexible control. Note that in the digital configuration, the input signal is greater than the voltage of the reference voltage. At that time the comparator changes states. The trip point can be adjusted by adjusting the W/L ratio. Every transistor has a W/L ratio that controls the threshold of the transistor.

Regarding claim 33 and 34, it is inherent that every comparator performs with hysteresis (or Schmitt trigger). When the W/L ratios of the transistors are not equal, the asymmetric Schmitt triggering happens. Because the threshold of the transistor is very low compared with the supply voltage, the time the comparator performs the digital configuration is longer (80% or more) comparing with the time the comparator in the analog configuration (input voltage is smaller than the threshold voltage).

Regarding claim 35, figure 11 of Ono shows a comparator having a comparator having trip points set corresponding to the W/L ratio of the components (transistors) of the circuit and the reference voltage (V_{ref}). Because the difference of the W/L ratios of the transistors of the circuit and the value of the reference voltage (external "trip point"), the "delay between the rising and falling edge transitions at an output signal of the comparator can be adjusted accordingly. If the level of the reference voltage is set to be low, the majority of the cycle time will be the digital configuration.

Regarding claims 36 and 37, the elements of the circuit of claim 36 are clearly shown in figure 11 of Ono. The pair of transistors are transistors (7) and (8). Figure 11 of Ono does not show inverters coupled to the output signal terminals. However, it is old and well known that inverters are used to invert a signal or used as buffers. Therefore, it would have been obvious to an artisan having skills in the art to implement inverters to the output terminal of the comparator to invert or to buffer the output signal. The load transistors comprise transistors (7) and (8).

Regarding claims 38-40, when the input voltage start to rise from ground level, the comparator in the analog configuration. When the input voltage is higher than the reference voltage, the output of the comparator changes state and the comparator is in the digital configuration. Depending on the level of the reference voltage, the cycle time of the digital configuration can be at a desired percentage.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hiep Nguyen whose telephone number is (571) 272-1752. The examiner can normally be reached on Monday to Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hiep Nguyen

06-15-05



TUAN T. LAM
PRIMARY EXAMINER